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High functionality reversible arithmetic logic unit

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ABSTRACT

Energy loss is a big challenge in digital logic design primarily due to impending end of Moore's Law. Increase in power dissipation not only affects portability but also overall life span of a device. Many applications cannot afford this loss. Therefore, future computing will rely on reversible logic for implementation of power efficient and compact circuits. Arithmetic and logic unit (ALU) is a fundamental component of all processors and designing it with reversible logic is tedious. The various ALU designs using reversible logic gates exist in literature but operations performed by them are limited. The main aim of this paper is to propose a new design of reversible ALU and enhance number of operations in it. This paper critically analyzes proposed ALU with existing designs and demonstrates increase in functionality with 56% reduction in gates, 17% reduction in garbage lines, 92% reduction in ancillary lines and 53% reduction in quantum cost. The proposed ALU design is coded in Verilog HDL, synthesized and simulated using EDA (Electronic Design Automation) tool-Xilinx ISE design suit 14.2. RCViewer+ tool has been used to validate quantum cost of proposed design.

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1. INTRODUCTION

Digital logic design based on conventional computing is getting obsolete due to high heat loss. In conventional computing based on irreversible logic; inputs cannot be predicted from output due to bit loss and therefore randomness is generated and that leads to heat loss [1]. By incorporating reversible logic in digital logic design, this heat loss can be avoided [2]. In reversible logic gates, number of output lines are mapped same as input lines to avoid bit loss and hence inputs can be easily recovered from output. ALU is an important building block of any digital logic design and find application in computers, smart phones, and digital signal processors etc. The initial research efforts in area of reversible logic based ALU was proposed by ancillary and garbage free V-shape design [3]. This design was proposed using only 6 elementary gates to perform 5 basic arithmetic and logical operations but there is scope of improvement of its functions [3]. A novel 5x5 Morrison gate [4] was used in designing of novel reversible ALU along with HNG gate. The Proposed circuit can perform nine arithmetic and logical operations. The quantum cost of proposed circuit is 35. The proposed circuit took two constant input lines and produced six garbage output lines. The first attempt to propose high functionality in ALU design was made by Guan and his coauthors. According to authors, their proposed circuit can perform 32 operations [5] but there are some redundant operations. A significant study by Syamala and Tilak [6] demonstrated two approaches of ALU Design. The first approach is control structure based reversible one-bit ALU design and another approach is

multiplexer based ALU design. The first approach is complex and slow in operation due to various control lines. Both proposed circuits have low functionality and high quantum cost.

Rakshith and Saligram [7] proposed improved fault tolerant reversible ALU that can perform 16 arithmetic and 16 logical operations. It is rather first effort of introducing high functionality along with fault tolerance property in ALU design. Optimized ALU circuit can be synthesized via 4*4 carry save adder [8]. Authors claimed significant improvement in quantum cost and gate count of their proposed ALU as compare to existing designs in literature. However, their proposed circuit is limited to only 8 arithmetic and logical operations. In reference paper [9] three designs of arithmetic and logic unit are proposed with significant improvement in functionality and quantum cost.

A modular approach for ALU design based on reversible multiplexer logic is proposed [10]. Authors proposed 1-bit ALU structure but unable to optimize quantum cost, ancillary inputs and garbage outputs. Proposed ALU performs 18 operations and has 59% inherent fault tolerance capability in QCA technology. The quantum cost of proposed circuit is undefined. Two ALU architectures are proposed based on Fredkin, Universal Reversible, Feynman, Toffoli and Peres Full adder gates [11]. The proposed circuit performs limited operations yet quantum cost is too high. Authors proposed ALU with high functionality and proposed ALU can be used for reversible programmable logic device [12].

Another ALU design is based on Feynman, Fredkin, HNG and PAOG gates but proposed circuit performs only six operations and not recommended for practical applications [13]. Another ALU structure is constructed using RUG gate and authors [14] proved their architecture area efficient as compare to other existing but quantum cost and other optimization aspects of reversible logic synthesis are not optimized in this research work. A recent study reveals new approach to design a high performance fault tolerant reversible ALU using universal parity preserving gate (UPPG) [15] and claimed 32 operations performed by their proposed design. The quantum cost of proposed circuit is 77 and there are some redundant operations in mentioned list. Proposed design has improved hardware complexity, gate count and quantum cost. Authors put forward two novel approaches for 1 bit reversible ALU design using elementary quantum gates and claim a significant contribution in reduction of quantum cost [16]. Their proposed designs have lowest quantum cost 24 for 12 operations but no architecture is discussed. Only quantum implementation is represented to claim quantum cost.

The comparative analysis and implementation of all significant research contributions in existing architectures is reported [17]. In research work [18], authors proposed two approaches of ALU design. One approach is based on their proposed gate and fault tolerant and other is based on combination of existing gates and their proposed gate.In second approach, complete ALU is not satisfying fault tolerance as Toffoli gate is not having this property. ALU based on both approaches perform 18 operations. WG gate can be utilized as full adder and subtractor in ALU circuits [19]. In research work reported in paper [20], authors proposed fault tolerant ALU for 12 operations but quantum cost is too high. Bahadori et al. [21] proposed a control unit with incorporated fault tolerance. Control unit performs 11 operations with quantum cost 24. The quantum cost of complete ALU is not discussed by authors. The research work reported in [22] performs 12 arithmetic and logic operations with 31 quantum cost. A novel reversible DSG gate and its quantum implementation is presented to implement high functionality ALU [23]. Improved fault tolerant ALU architecture with 73 operations is claimed in research work [24]. ALU design with QCA implementation is presented in research work [25].

Above literature survey show that researchers have done significant work in area of reversible logic based ALU design. Optimization is an intractable problem and there is still lot of scope to improve functionality and quantum cost for improving overall performance of reversible logic based ALU. This paper presents novel architecture of ALU with high functionality. Summary of all reversible logic gates used in proposed novel reversible ALU architecture is presented in Table 1. Methodology of proposed work is explained in section 2. Proposed design is given in section 3. Performance evaluation is given in section 4 followed by conclusion in section 5.

Table 1. Reversible gates used in proposed architecture

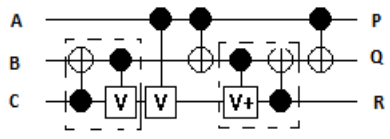
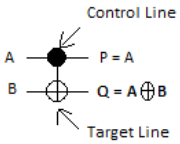
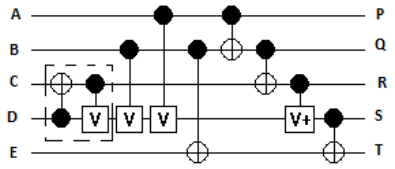
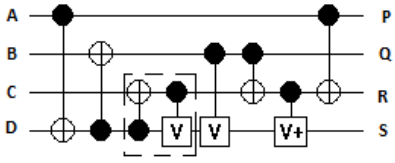
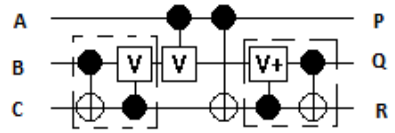
Reversible Gate	Logic Implemented	QC	NCT/NCV Equivalence
Fredkin (FR)	$P = A$ $Q = \bar{A}B \oplus AC$ $R = \bar{A}C \oplus AB$	5	

Table 1. Reversible gates used in proposed architecture (*continue*)

Reversible Gate	Logic Implemented	QC	NCT/NCV Equivalence
Feynman	P = A Q = A⊕B	1	
Fault Tolerant Reversible Adder(FTRA)	P = A Q = B R = A⊕B⊕C⊕D S = (A⊕B)(C⊕D)⊕(AB⊕D) T = (A⊕B)(C⊕D)⊕(ĀB⊕D)⊕E	8	
WG	P = A Q = A⊕B⊕D R = A⊕B⊕C S = (A⊕D)(B+C) + BC	7	
RMUX1	P = A Q = ĀB+AC R = ĀC + AB̄	4	

2. RESEARCH METHOD

The proposed novel reversible ALU is designed using 7 reversible logic based gates including one WG gate [19], one FTRA gate, three RMUX1 gates, one Feynman gate and one Fredkin gate. Proposed ALU design is shown in Figure 1. FTRA gate is 5*5 parity preserving fault tolerant reversible adder gate which can work as full adder as well as full subtractor along with performing other logical operations; proving it to be a universal logic gate. FTRA gate is operated under various combinations of selection lines to perform 13 logical operations. Logical operations XOR, XNOR, A=B are obtained on F1 output line, AND, NOR, OR, NAND are obtained on F2 line and (A+B'), (A'+B), AB', A'B, A>B, A<B are obtained on F3 output line. Functionality of FTRA gate under various combinations of S0, S1, and S2 is shown in Table 2.

Table 2. Functionality of FTRA gate

S2	S1	S0	F1	F2	F3
0	0	0	XOR	AND	A<B
0	0	1	XOR	AND	A+B'
0	1	0	XNOR	NOR	A'+B
0	1	1	XNOR	NOR	A>B
1	0	0	A=B	OR	AB'
1	1	1	XOR	NAND	A'B

RMUX1 gate (1) is acting as multiplexer. It selects F1 or F2 based on selection line S3 and provides it on output line T3. Functionality of RMUX1 gate (1) is shown in Table 3. If S3 is 0, then F1 is passed on T3 output line, otherwise F2 is passed. RMUX1 gate (2) is acting as multiplexer. It selects T3 (F1 or F2) or F3 based on selection line S4 and provides it on output line T4. Functionality of RMUX1 gate (2) is shown in Table 4. When S4 is 0 then T3 is passed on T4 output line. It means if S3 =0, S4=0, Then F1 is passed on T4 output line. If S3=1 and S4=0, then F2 is passed on T4 output line. When S4 is 1, then F3 is passed on T4 output line. Feynman gate is used to avoid fan out and it generates two copies of T4 on T5 and Desired logical function line (FuncL). Fredkin gate is passing T5 or Cin/Bin based on selection line S5. Functionality of Fredkin gate is shown in Table 5. If S5 is 0, then T5 is passed On T6 output line otherwise initial carry or borrow i.e. Cin or Bin is passed on output line.

Table 3. Functionality of RMUX1 gate (1)

S3	T3
0	F1
1	F2

Table 4. Functionality of RMUX1 gate (2)

S4	T4
0	T3
1	F3

Table 5. Functionality of fredkin gate

S5	T6
0	T5
1	Cin/Bin

WG gate is acting as full adder or subtractor based on control line AS. If input vector of WG gate is considered as A,B,C,D and output vector is considered as P,Q,R,S then WG gate works as full adder with three inputs A,B and Cin are provided on A,B,C lines and D(AS) is put to zero. In this arrangement, sum is obtained on R line and Cout is obtained on S line. While for subtraction inputs A, B and Bin are provided on A, B and C lines respectively and D (AS) is put to one. In this arrangement, Difference is obtained on R line and Bout is obtained on S line. The desired arithmetic operations are obtained on FuncA output line. Functionality of WG gate is shown in Table 6. If AS=0, then arithmetic addition takes place otherwise arithmetic subtraction takes place. RMUX1 gate (3) is acting as multiplexer. It selects FuncL or FuncA based on control line AL and provides it on output line Func. Functionality of RMUX1 gate (3) is shown in Table 7. If AL=0, then logical operation is selected on Func output line otherwise arithmetic operation is selected.

Table 6. Functionality of WG gate

T1	T2	T6	AS	FuncA	Cout/Bout
A	B	Cin	0	A plus B plus Cin	Cout
A	B	Bin	1	A minus B minus Bin	Bout

Table 7. Functionality of RMUX1 gate (3)

AL	Func
0	FuncL
1	FuncA

3. PROPOSED DESIGN

The proposed novel reversible ALU is designed using 7 reversible logic based gates including one WG gate, one FTRA gate, three RMUX1 gates, one Feynman gate and one Fredkin gate. The quantum cost of proposed circuit is 33. Complete ALU is designed using 12 input lines including three input bits A(Operand1), B (Operand 2), Cin (Carry input)/Bin(Borrow input), one constant input line, five selection lines to select logical operation and two control lines to choose between logical and arithmetic and further addition or subtraction. The designed circuit uses 12 output lines including 10 garbage output lines, one desired Func line and Cout(Carry output)/Bout(Borrow output). The proposed circuit generates 10 garbage outputs and utilizes only one ancillary input line to maintain reversibility. The main advantage of the proposed ALU design is its high functionality with lowest quantum cost. The proposed ALU design is shown in Figure 1. The simulation waveform for proposed ALU is shown in Figure 2.

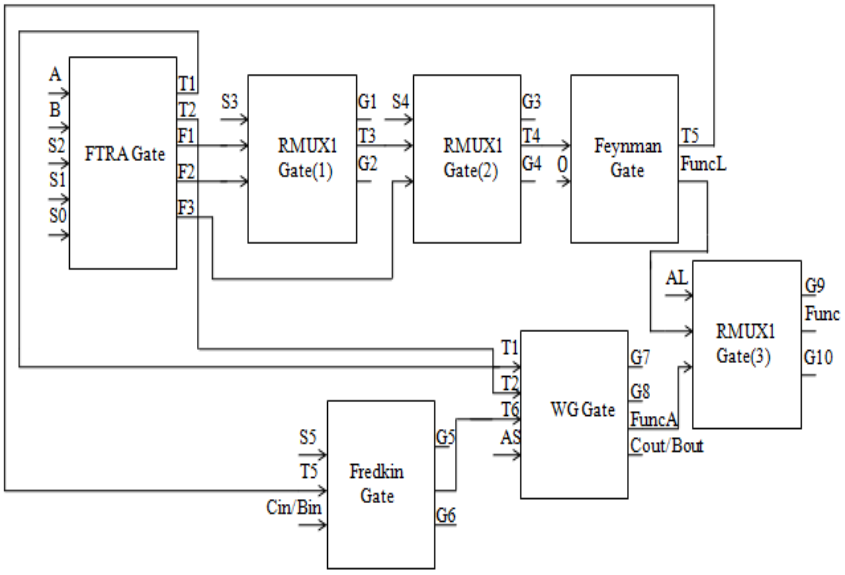


Figure 1. Proposed novel reversible ALU architecture

The proposed circuit is able to perform 35 operations including 13 logical and 22 arithmetic operations as shown in Table 8. The symbol '*' in table indicates don't care means either 0 or 1 can be assigned to corresponding position in which '*' is marked. AL=0 indicates desired operation is logical otherwise it is arithmetic. AS=0 indicates desired arithmetic operation is addition otherwise it is subtraction. The logical operator '+' is used for OR operation and arithmetic operator 'plus' is used for addition and 'minus' is used for subtraction.

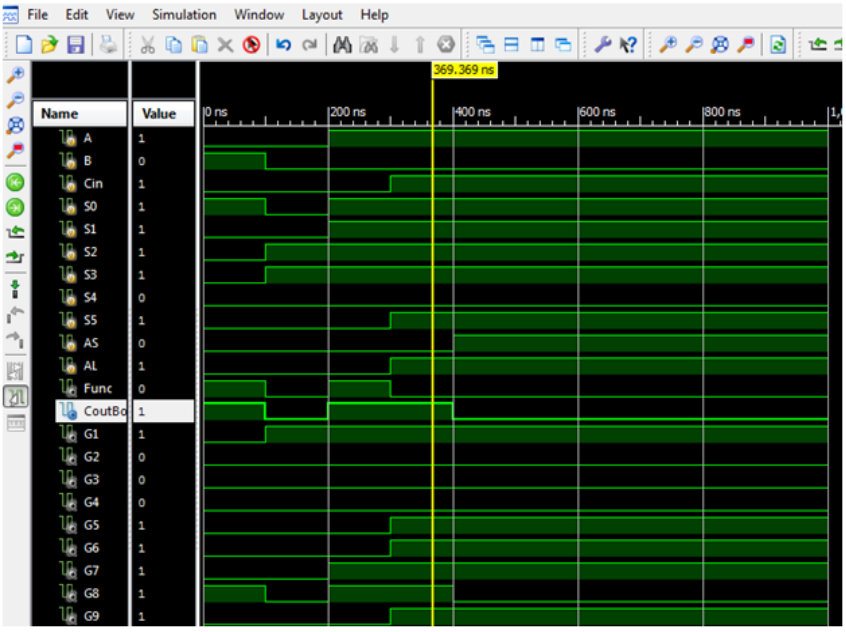


Figure 2. Simulation waveform of proposed ALU

Table 8. Operations performed by proposed ALU

S4	S3	S2	S1	So	uncL (S5=*,AS=*, AL=0)	FuncA1 (S5=0, AS=0,AL=1)	FuncA2 (S5=0, AS=1, AL=1)
0	0	0	0	1	A XOR B	A plus B plus (A XOR B)	A minus B minus (A XOR B)
0	1	0	0	1	A AND B	A plus B plus AB	A minus B minus AB
1	*	0	0	1	A+B'	A plus B plus (A+B')	A minus B minus (A+B')
0	0	0	1	0	A XNOR B	A plus B plus (A XNOR B)	A minus B minus (A XNOR B)
0	1	0	1	0	A NOR B	A plus B plus (A'.B')	A minus B minus (A'.B')
1	*	0	1	0	A'+B	A plus B plus (A'+B)	A minus B minus (A'+B)
0	1	1	0	0	A OR B	A plus B plus (A+B)	A minus B minus (A+B)
1	*	1	0	0	AB'	A plus B plus (AB')	A minus B minus (AB')
0	1	1	1	1	A NAND B	A plus B plus (A'+B')	A minus B minus (A'+B')
1	*	1	1	1	A'B	A plus B plus A'B	A minus B minus A'B
1	*	0	1	1	A>B	FuncA1	FuncA2
0	0	1	0	0	A=B	(S5=1, AS=0,AL=1)	(S5=1, AS=1,AL=1)
1	*	0	0	0	A<B		
*	*	*	*	*		A plus B plus Cin	A minus B minus Bin

4. PERFORMANCE EVALUATION

The performance evaluation of existing designs and proposed ALU architecture is done in terms of functionality, quantum cost, gate count, garbage outputs and ancillary inputs. Highest number of operations reported in cited literature [5, 7, 15] is 32 yet operations performed by proposed architecture are 35. The proposed circuit is designed with only seven reversible logic based gates yet minimum count reported in cited literature [18] is 11. Proposed ALU architecture took only one constant input lines yet minimum count reported in literature [18] is 7. Proposed circuit produces 10 garbage output lines yet minimum count reported in cited literature [5] is 12. The minimum quantum cost reported in cited literature [5] is 70 yet quantum cost of proposed novel reversible ALU design is 33. The performance evaluation of various ALU designs is given in Table 9. Performance evaluation in terms of bar chart is given in Figure 3 for clear understanding and critical analysis.

Table 9. Performance evaluation

ALU Designs	Design I[5]	Design II[7]	Design III[15]	Design IV[18]	Proposed Design
No. of Gates	24	17	16	11	7
Quantum Cost	70	595	77	99	33
Arithmetic & Logic Operations	32	32	32	18	35
Garbage Outputs	12	37	25	22	10
Ancillary Inputs	12	33	25	7	1
Fault Tolerance	No	Yes	Yes	No	No

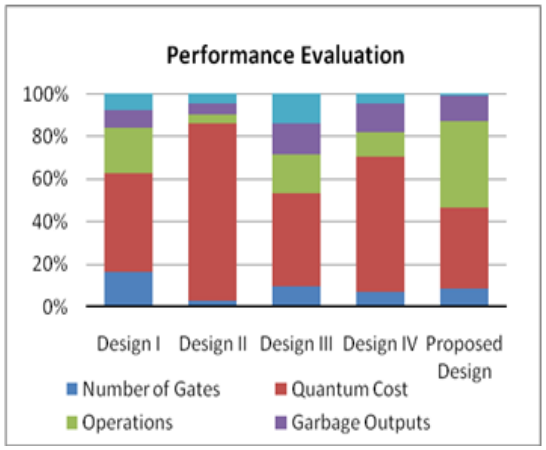


Figure 3. Performance evaluation of novel reversible ALU

5. CONCLUSION

The proposed ALU architecture has two major advantages over existing designs. Firstly, it produces more arithmetic and logical calculations and proves significant improvement in functionality. Secondly, quantum cost of proposed circuit is least among all architectures. The designed architecture is based on divide and conquers approach. Complete ALU design is splitted into two sections. One is dedicated logical block and performs 13 logical operations. Other is dedicated arithmetic block and performs 22 arithmetic operations. Control unit is designed using multiplexer which selects desired operation as per logic needed. The proposed design demonstrates increase in functionality with 56% reduction in gates, 17% reduction in garbage lines, 92% reduction in ancillary lines and 53% reduction in quantum cost. Future scope of this research is to embed multiplier and divider along with other arithmetic operations.

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